CMS80F262x Datasheet

Enhanced 1T 8051 microcontroller with flash memory

Rev. 1.0.4

1. Product Features

1.1 Features

- **Compatible with MCS-51 1T Instruction System**
  - System clock frequency supports up to 48MHz
  - Machine cycle maximum $1T_{SYS}$ @ F_{SYS}=24MHz
  - Machine cycle maximum $2T_{SYS}$ @ F_{SYS}=48MHz
- **Memory**
  - Program FLASH: 64K×8Bit
  - Data FLASH: 1K×8Bit
  - General RAM: 256×8Bit
  - Universal XRAM: 4K×8Bit
  - Program FLASH supports partition protection and IAP
  - Data FLASH supports partition protection
- **4 Oscillation Modes**
  - HSI-Internal high-speed oscillator: 48MHz
  - HSE-External high-speed oscillator: 8MHz/16MHz
  - LSE-External low-speed oscillator: 32.768KHz
  - LSI-Internal low-speed oscillator: 125KHz
- **GPIO**
  - Up to 46 GPIOs
  - Support pull-up/down resistor function
  - Support edge (rising edge/falling edge/both edge) interrupt
  - Support wake-up function
- **Interrupt Source**
  - Support all external port interrupts
  - Up to 8 timer interrupts
  - Other peripheral interrupts
- **Timer**
  - WDT/WWDT timer (watchdog/ window watchdog timer)
  - Up to 5 timers: Timer0/1, Timer2, Timer3/4
  - LSE Timer (support sleep wake function)
  - WUT (wake-up timer)
  - BRT/ BRT1 (baud rate clock generation timer)
- **Cyclic Redundancy Check Unit**
  - CRC16 (CRC16-CCITT)
- **Multiplication and Division Operation Unit (MDU)**
  - Support 32bit/16bit, 16bit/16bit, 16bit×16bit
- **Buzzer Driver**
  - 50% duty cycle, frequency can be set freely
- **Enhanced PWM**
  - 6 channels enhanced PWM
  - 6 independent cycle counters
  - Support independent /complementary/ synchronous/ group mode
  - Support edge alignment/center alignment
  - Support complementary mode dead zone delay function
  - Support mask function and fault protection function
- **Operating Voltage Range**
  - 2.1V ~ 5.5V
- **Operating Temperature Range**
  - -40℃ ~ 105℃
- **Low-voltage Reset Function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low-voltage Detection Function (LVD)**
  - 2.0V ~ 4.6V, 16 levels optional
- **High-precision 12-bit ADC**
  - Up to 23 AD external channels
  - Optional reference voltage (2.0V/2.4V/3.0V/VDD)
  - Can detect internal 1.2V reference voltage
  - Support hardware trigger start conversion function
  - Support a set of result digital comparison function
- **Hardware LCD Driver**
  - Optional duty cycle: 1/4, 1/5, 1/6, 1/8
  - Optional three clock sources: LSI/LSE/system clock
  - Traditional resistive LCD, optional BIAS: 1/2, 1/3, 1/4
  - Support work in sleep mode
  - Support fast charging mode
  - Support energy-saving mode, the total resistance of voltage divider can be 60K/225K/900K
  - Support up to 4COM x 36SEG, 5COM x 35SEG 6COM x 34SEG, 8COM x 32SEG
- **Hardware LED Driver**
  - Optional duty cycle: 1/4, 1/5, 1/6, 1/8
  - Support two modes: common cathode/common anode
  - Optional three clock sources: LSI/LSE/system clock
  - Optional COM, SEG current
  - Support up to 4COM x 28SEG, 5COM x 27SEG 6COM x 26SEG, 8COM x 24SEG
- **Two Analog Comparators (ACMP0/1)**
  - 5 options for the positive terminal, internal 1.2V/VDD divider for the negative terminal
  - Comparator supports unilateral/bilateral hysteresis
  - Optional hysteresis voltage 10/20/60mV
  - Support comparison output trigger EPWM brake
  - The internal 1.2V/VDD divider of the negative terminal can be connected to the internal ADC channel
  - Supports output latching
- **Low Power Mode**
  - Idle mode 1/2
  - Sleep mode (STOP)
- **Support Two-wire Serial Programming and Debugging**

- **Communication Module**
  - 1xSPI (communication rate up to 6Mb/s)
  - 1xI2C (communication rate up to 400Kb/s)
  - Up to 4xUART (baud rate up to 1Mb/s)
- **Support 96-bit Unique ID Number (UID)**
  - Each chip has an independent ID number

1.2 Product Comparison

Peripherals \ Product		CMS80F26282	CMS80F2629	CMS80F262A	CMS80F262B	CMS80F262C
Maximum clock frequency		48MHz				
Memory size	APROM	64				
	Data FLASH	1 KB				
	RAM	256 B				
	XRAM	4 KB				
Timer	WDT	1				
	WWDT	1				
	Timer0/1	2 (16bit)				
	Timer2	1 (16bit)				
	Timer3/4	2 (16bit)				
	LSE_Timer	1 (16bit)				
	WUT	1 (12bit)				
	BRT/BRT1	2 (16bit)				
Enhanced digital peripherals	CRC	CRC16-CCITT				
	MDU	32bit/16bit, 16bit/16bit, 16bit*16bit				
	BUZZER	1				
	PWM	6(16bit)				
Display interface	LCD	4COM x 16SEG 5COM x 15SEG 6COM x 14SEG 8COM x 12SEG	4COM x 20SEG 5COM x 19SEG 6COM x 18SEG 8COM x 16SEG	4COM x 32SEG 5COM x 31SEG 6COM x 30SEG 8COM x 28SEG	4COM x 36SEG 5COM x 35SEG 6COM x 34SEG 8COM x 32SEG	4COM x 32SEG 5COM x 31SEG 6COM x 30SEG 8COM x 28SEG
	LED	4COM x 14SEG 5COM x 13SEG 6COM x 12SEG 8COM x 10SEG	4COM x 17SEG 5COM x 16SEG 6COM x 15SEG 8COM x 13SEG	4COM x 28SEG 5COM x 27SEG 6COM x 26SEG 8COM x 24SEG	4COM x 28SEG 5COM x 27SEG 6COM x 26SEG 8COM x 24SEG	4COM x 28SEG 5COM x 27SEG 6COM x 26SEG 8COM x 24SEG
Communication	SPI	1				
	I2C	1				
	UART	2	2	4	4	4
Analog	12bit-ADC (Number of external channels)	14	16	23	23	19
	ACMP	2	2	2	2	2
GPIOs		26	30	42	46	38
LVR		1.8V/2.0V/2.5V/3.5V				
LVD		2.0V ~ 4.6V, 16 levels optional				
Operating voltage		2.1 ~ 5.5 V				
Operating temperature		-40 ~ 105℃				
Package		SOP28	LQFP32	LQFP44	LQFP48	QFN40

2. System Overview

2.1 System Introduction

CMS80F262x series is an 8051 core, a 1T instruction system compatible with MCS-51, and a general IO type 8-bit chip. The operating frequency can reach up to 48MHz. The MCU has the following characteristics:

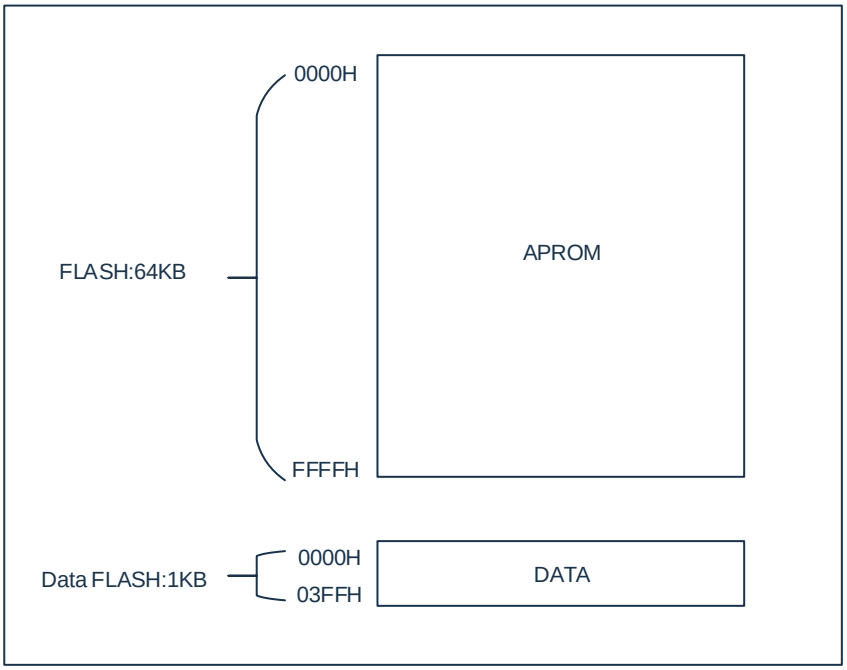
- With 64KB program area, 256B RAM space, 4KB XRAM, 1KB Data FLASH area.
- With four oscillation modes.
- It supports four working modes: normal, idle 1, idle 2, and sleep, which can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage detection LVD, watchdog overflow reset, window watchdog reset and other protection settings can effectively improve the reliability of system operation.
- With multiple interrupt sources such as external interrupts, timer interrupts and other peripheral interrupts, it can respond to external events in a timely manner and improve the utilization of the MCU.
- 11 timers, which can realize functions such as timing, counting, input capture, output comparison, timing wake-up, and baud rate generator.
- With hardware multiplication and division unit MDU, cyclic redundancy check unit CRC.
- LED driver module supports up to 8COM and 24SEG.
- LCD driver module supports up to 8COM and 32SEG.
- 6-channel 16-bit PWM, supports independent, complementary, and synchronous three-mode output, and has hardware brake function, dead zone control function, mask output and other functions.
- With 1 I2C, 1 SPI, and 4 UART communication modules, it can realize data transmission between the system and other devices.
- With high-precision 12-bit ADC and selectable internal reference voltage, up to 2 comparators, and more abundant analog functions.

2.2 Memory Structure

2.2.1 Program Memory FLASH

This series has 64KB FLASH storage space.

The block diagram of the FLASH space allocation structure is as follows:

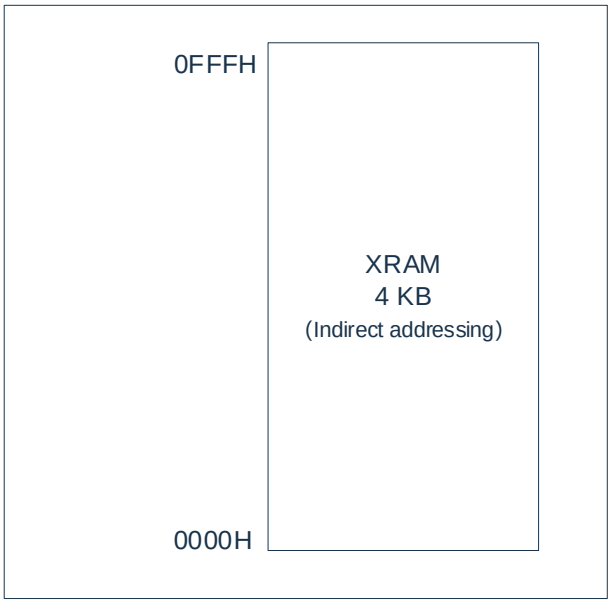


2.2.2 Internal Data Memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The structure diagram of RAM space allocation is shown in the figure below:

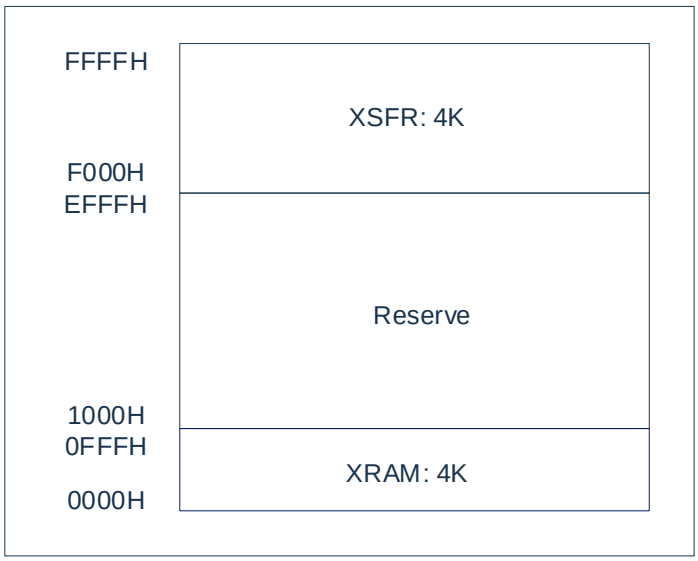
2.2.3 External Data Memory XRAM

There is 4KB XRAM area inside the chip, which is not related to RAM/FLASH. The structure diagram of XRAM space allocation is shown in the figure below.



2.2.4 Special Function Register XSFR

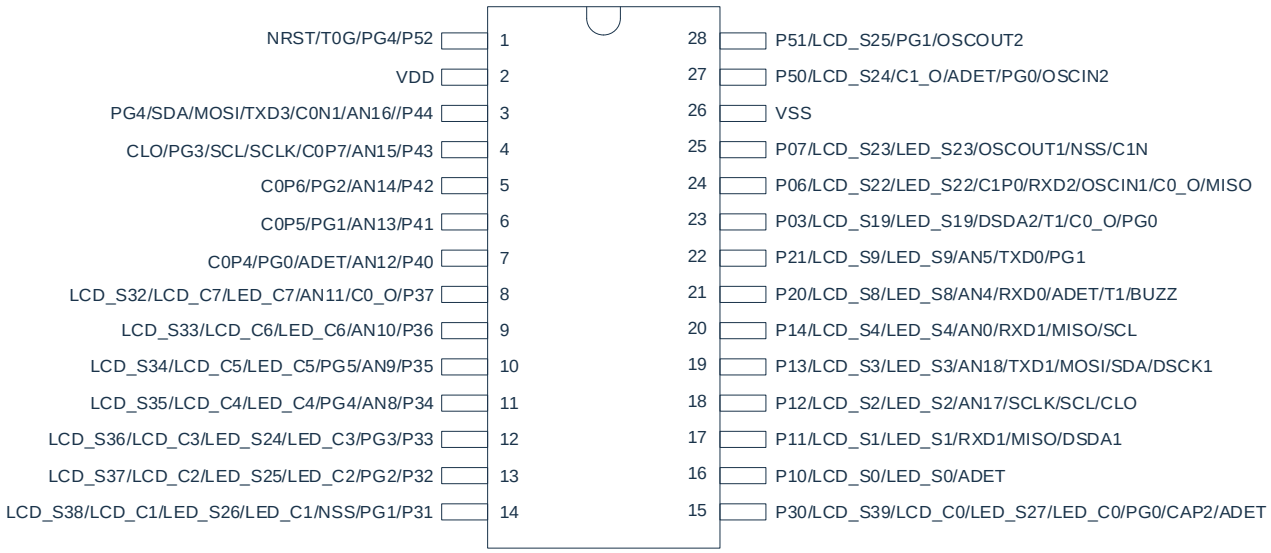
XSFR is a special register shared by the addressing space of XRAM, which mainly includes port control register and other function control registers. Its addressing range is as follows:



3. Pin Assignment

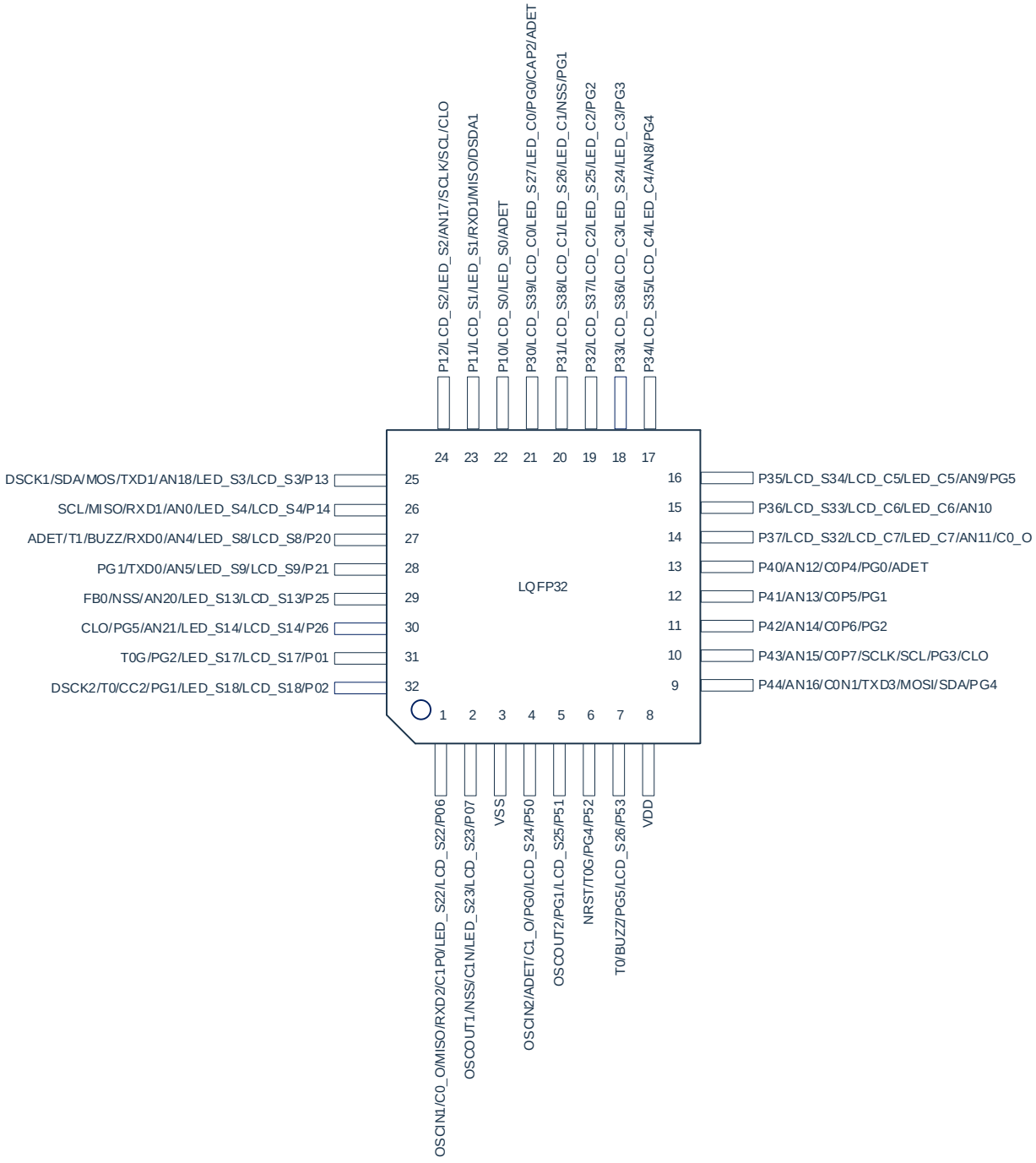
3.1 Pin Description

3.1.1 CMS80F26282 Pin Diagram

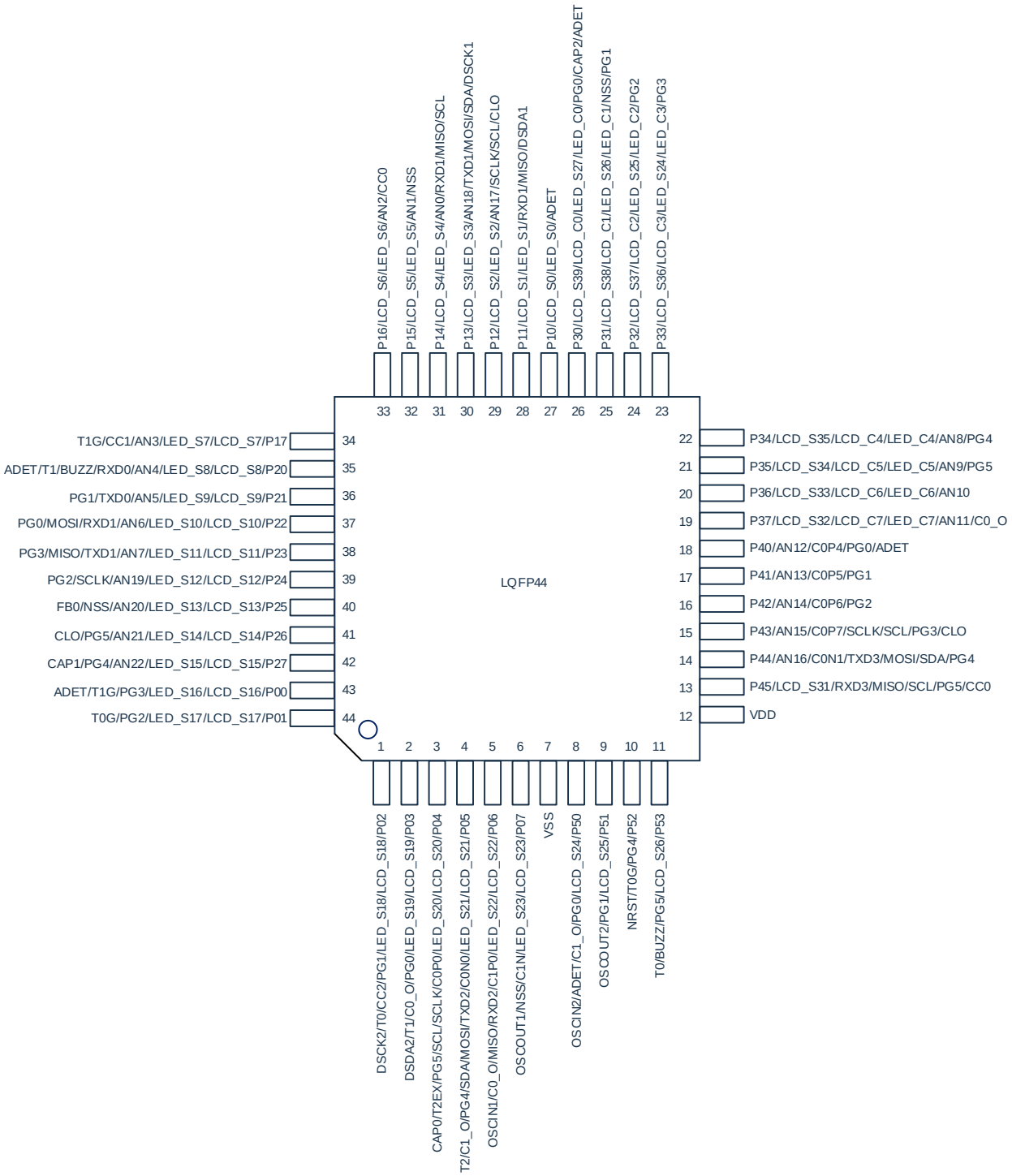


CMS80F26282-SOP28

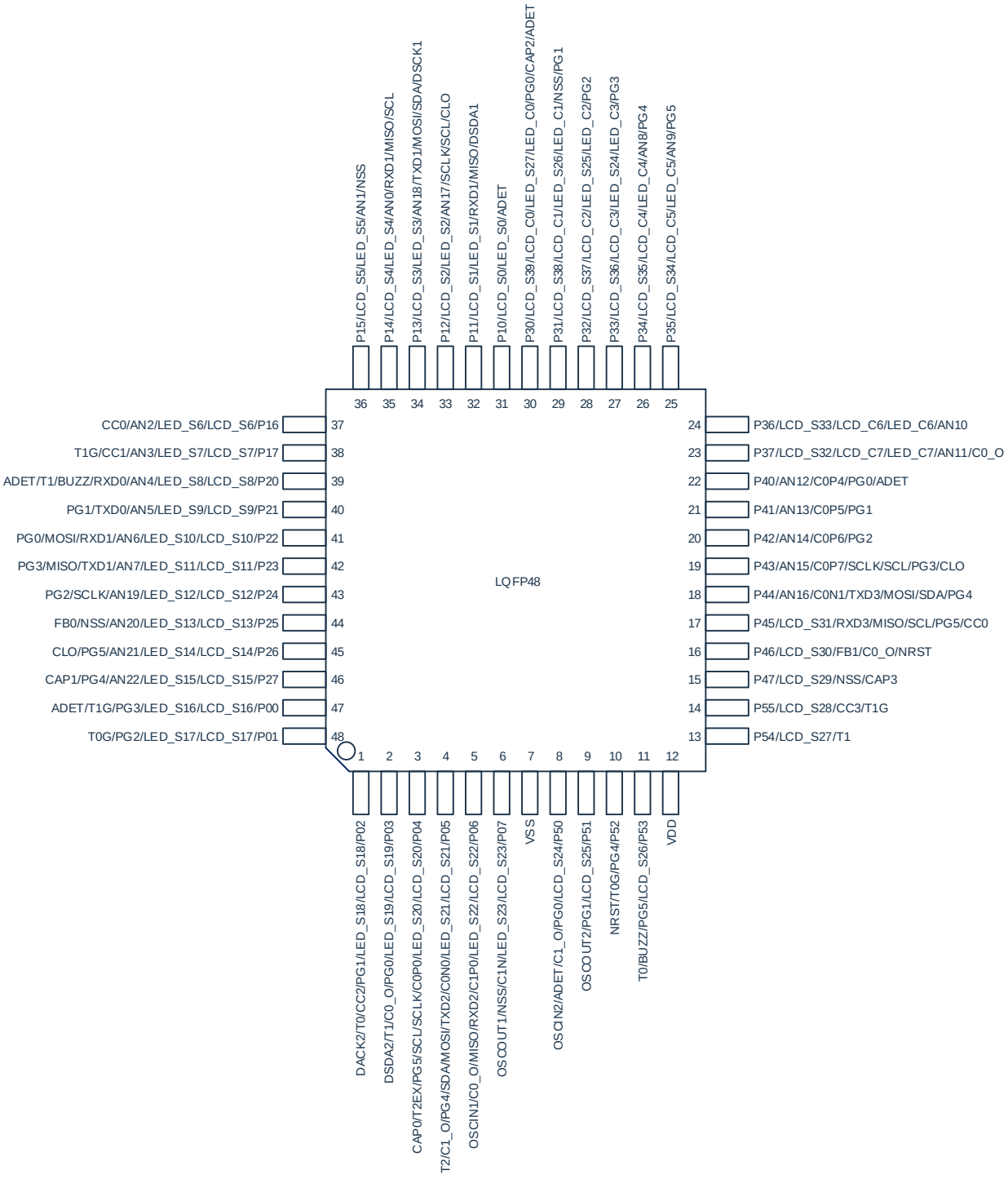
3.1.2 CMS80F2629 Pin Diagram



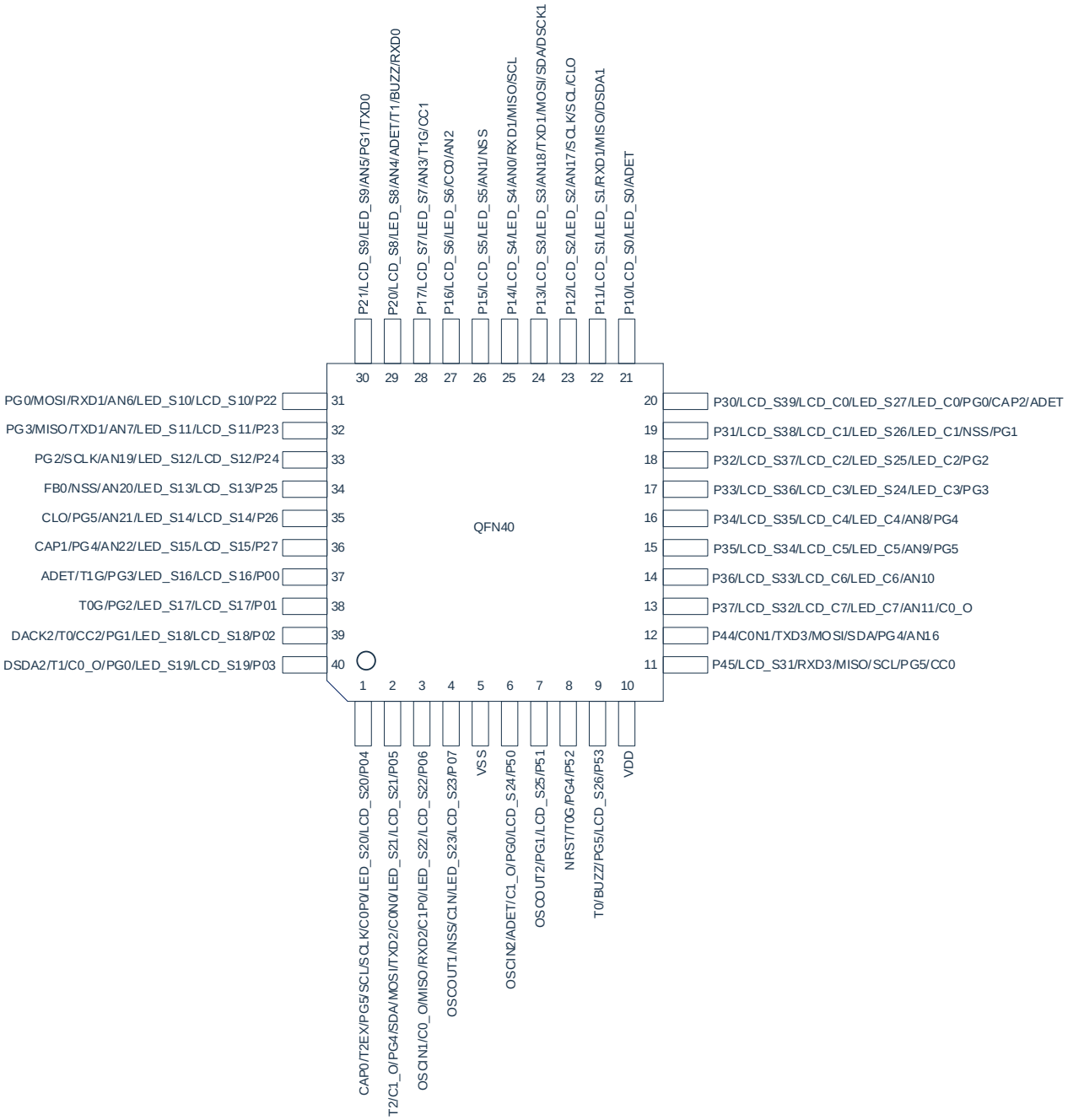
3.1.3 CMS80F262A Pin Diagram



3.1.4 CMS80F262B Pin Diagram



3.1.5 CMS80F262C Pin Diagram



3.2 Pin Description

Symbol description: I/O digital input or output, I digital input, O digital output, AI analog input, AO analog output.

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
-	-	43	47	37	P00	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S16	AO	LCD SEG16 output
					LED_S16	O	LED SEG16 output
					PG3	O	PWM output channel 3
					T1G	I	Timer1 gate control input
					ADET	I	ADC external trigger input
-	31	44	48	38	P01	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S17	AO	LCD SEG17 output
					LED_S17	O	LED SEG17 output
					PG2	O	PWM output channel 2
					T0G	I	Timer0 gate control input
-	32	1	1	39	P02	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S18	AO	LCD SEG18 output
					LED_S18	O	LED SEG18 output
					PG1	O	PWM output channel 1
					CC2	O	Timer2 comparison output channel 2
					T0	I	Timer0 external clock input
					DSCK2	I/O	Programming and debugging clock input and output
23	-	2	2	40	P03	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S19	AO	LCD SEG19 output
					LED_S19	O	LED SEG19 output
					PG0	O	PWM output channel 0
					C0_O	O	ACMP0 output
					T1	I	Timer1 external clock input
					DSDA2	I/O	Programming and debugging data input and output
-	-	3	3	1	P04	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S20	AO	LCD SEG20 output
					LED_S20	O	LED SEG20 output
					C0P0	AI	ACMP0 positive input channel 0
					SCLK	I/O	SPI clock input and output
					SCL	I/O	I^2C clock input and output

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					PG5	O	PWM output channel 5
					T2EX	I	Timer2 fall edge automatic reload input
					CAP0	I	Timer2 input capture channel 0
-	-	4	4	2	P05	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S21	AO	LCD SEG21 output
					LED_S21	O	LED SEG21 output
					C0N0	AI	ACMP0 negative input channel 0
					TXD2	O	UART2 data output
					MOSI	I/O	SPI master send and slave receive
					SDA	I/O	I^2C data input and output
					PG4	O	PWM output channel 4
					C1_O	O	ACMP1 output
					T2	I	Timer2 external events or gate control input
24	1	5	5	3	P06	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S22	AO	LCD SEG22 output
					LED_S22	O	LED SEG22 output
					C1P0	AI	ACMP1 positive input channel 0
					RXD2	I/O	UART2 data input or synchronous mode data output
					MISO	I/O	SPI master receive and slave send
					C0_O	O	ACMP0 output
					OSCIN1	AI	External oscillation 1 input
25	2	6	6	4	P07	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S23	AO	LCD SEG23 output
					LED_S23	O	LED SEG23 output
					C1N	AI	ACMP1 negative input
					NSS(NSSO0)	I/O	SPI slave select input or master select channel 0 output
					OSCOUT1	AO	External oscillation 1 output
16	22	27	31	21	P10	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S0	AO	LCD SEG0 output
					LED_S0	O	LED SEG0 output
					ADET	I	ADC external trigger input
17	23	28	32	22	P11	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S1	AO	LCD SEG1 output

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					LED_S1	O	LED SEG1 output
					RXD1	I/O	UART1 data input or synchronous mode data output
					MISO	I/O	SPI master receive and slave send
					DSDA1	I/O	Programming and debugging data input and output
18	24	29	33	23	P12	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S2	AO	LCD SEG2 output
					LED_S2	O	LED SEG2 output
					AN17	AI	ADC input channel 17
					SCLK	I/O	SPI clock input and output
					SCL	I/O	I^2C clock input and output
					CLO	O	System clock division output
19	25	30	34	24	P13	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S3	AO	LCD SEG3 output
					LED_S3	O	LED SEG3 output
					TXD1	O	UART1 data output
					AN18	AI	ADC input channel 18
					MOSI	I/O	SPI master send and slave receive
					SDA	I/O	I^2C data input and output
					DSCK1	I/O	Programming and debugging clock input and output
20	26	31	35	25	P14	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S4	AO	LCD SEG4 output
					LED_S4	O	LED SEG4 output
					AN0	AI	ADC input channel 0
					RXD1	I/O	UART1 data input or synchronous mode data output
					MISO	I/O	SPI master receive and slave send
					SCL	I/O	I^2C clock input and output
-	-	32	36	26	P15	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S5	AO	LCD SEG5 output
					LED_S5	O	LED SEG5 output
					AN1	AI	ADC input channel 1
					NSS(NSSO1)	I/O	SPI slave select input or master select channel 1 output
-	-	33	37	27	P16	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S6	AO	LCD SEG6 output

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					LED_S6	O	LED SEG6 output
					AN2	AI	ADC input channel 2
					CC0	O	Timer2 comparison output channel 0
-	-	34	38	28	P17	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S7	AO	LCD SEG7 output
					LED_S7	O	LED SEG7 output
					AN3	AI	ADC input channel 3
					CC1	O	Timer2 comparison output channel 1
					T1G	I	Timer1 gate control input
21	27	35	39	29	P20	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S8	AO	LCD SEG8 output
					LED_S8	O	LED SEG8 output
					AN4	AI	ADC input channel 4
					RXD0	I/O	UART0 data input or synchronous mode data output
					BUZZ	O	Buzzer output
					T1	I	Timer1 external clock input
					ADET	I	ADC external trigger input
22	28	36	40	30	P21	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S9	AO	LCD SEG9 output
					LED_S9	O	LED SEG9 output
					AN5	AI	ADC input channel 5
					TXD0	O	UART0 data output
					PG1	O	PWM output channel 1
-	-	37	41	31	P22	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S10	AO	LCD SEG10 output
					LED_S10	O	LED SEG10 output
					AN6	AI	ADC input channel 6
					RXD1	I/O	UART1 data input or synchronous mode data output
					MOSI	I/O	SPI master send and slave receive
					PG0	O	PWM output channel 0
-	-	38	42	32	P23	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S11	AO	LCD SEG11 output
					LED_S11	O	LED SEG11 output

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					AN7	AI	ADC input channel 7
					TXD1	O	UART1 data output
					MISO	I/O	SPI master receive and slave send
					PG3	O	PWM output channel 3
-	-	39	43	33	P24	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S12	AO	LCD SEG12 output
					LED_S12	O	LED SEG12 output
					AN19	AI	ADC input channel 19
					SCLK	I/O	SPI clock input and output
					PG2	O	PWM output channel 2
-	29	40	44	34	P25	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S13	AO	LCD SEG13 output
					LED_S13	O	LED SEG13 output
					AN20	AI	ADC input channel 20
					NSS(NSSO2)	I	SPI slave select input or master select channel 2 output
					FB0	I	PWM external brake signal 0 input
-	30	41	45	35	P26	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S14	AO	LCD SEG14 output
					LED_S14	O	LCD SEG14 output
					AN21	AI	ADC input channel 21
					PG5	I	PWM output channel 5
					CLO	O	System clock division output
-	-	42	46	36	P27	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S15	AO	LCD SEG15 output
					LED_S15	O	LED SEG15 output
					AN22	AI	ADC input channel 22
					PG4	I	PWM output channel 4
					CAP1	I	Timer2 input capture channel 1
15	21	26	30	20	P30	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S39	AO	LCD SEG39 output
					LCD_C0	AO	LCD COM0 output
					LED_S27	O	LED SEG27 output
					LED_C0	O	LED COM0 output
					PG0	I	PWM output channel 0

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					CAP2	I	Timer2 input capture channel 2
					ADET	I	ADC external trigger input
14	20	25	29	19	P31	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S38	AO	LCD SEG38 output
					LCD_C1	AO	LCD COM1 output
					LED_S26	O	LED SEG26 output
					LED_C1	O	LED COM1 output
					PG1	I	PWM output channel 1
					NSS(NSSO3)	I/O	SPI slave select input or master select channel 3 output
13	19	24	28	18	P32	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S37	AO	LCD SEG37 output
					LCD_C2	AO	LCD COM2 output
					LED_S25	O	LED SEG25 output
					LED_C2	O	LED COM2 output
					PG2	I	PWM output channel 2
12	18	23	27	17	P33	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S36	AO	LCD SEG36 output
					LCD_C3	AO	LCD COM3 output
					LED_S24	O	LED SEG24 output
					LED_C3	O	LED COM3 output
					PG3	I	PWM output channel 3
11	17	22	26	16	P34	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S35	AO	LCD SEG35 output
					LCD_C4	AO	LCD COM4 output
					LED_C4	O	LED COM4 output
					AN8	AI	ADC input channel 8
					PG4	I	PWM output channel 4
10	16	21	25	15	P35	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S34	AO	LCD SEG34 output
					LCD_C5	AO	LCD COM5 output
					LED_C5	O	LED COM5 output
					AN9	AI	ADC input channel 9
					PG5	I	PWM output channel 5
9	15	20	24	14	P36	I/O	GPIO configures input, output, pull-

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
							up, pull-down and other functions through registers
					LCD_S33	AO	LCD SEG33 output
					LCD_C6	AO	LCD COM6 output
					LED_C6	O	LED COM6 output
					AN10	AI	ADC input channel 10
8	14	19	23	13	P37	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S32	AO	LCD SEG32 output
					LCD_C7	AO	LCD COM7 output
					LED_C7	O	LED COM7 output
					AN11	AI	ADC input channel 11
					C0_O	O	ACMP0 output
7	13	18	22	-	P40	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					AN12	AI	ADC input channel 12
					C0P4	AI	Comparator 0 positive input channel 4
					PG0	O	PWM output channel 0
					ADET	I	ADC external trigger input
6	12	17	21	-	P41	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					AN13	AI	ADC input channel 13
					C0P5	AI	Comparator 0 positive input channel 5
					PG1	O	PWM output channel 1
5	11	16	20	-	P42	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					AN14	AI	ADC input channel 14
					C0P6	AI	Comparator 0 positive input channel 6
					PG2	O	PWM output channel 2
4	10	15	19	-	P43	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					AN15	AI	ADC input channel 15
					C0P7	AI	Comparator 0 positive input channel 7
					SCLK	I/O	SPI clock input and output
					SCL	I/O	I^2C clock input and output
					PG3	O	PWM output channel 3
					CLO	O	System clock division output
3	9	14	18	12	P44	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					AN16	AI	ADC input channel 16
					C0N1	AI	ACMP0 negative input channel 1
					TXD3	O	UART3 data output
					MOSI	I/O	SPI master send and slave receive
					SDA	I/O	I^2C data input and output
					PG4	O	PWM output channel 4
-	-	13	17	11	P45	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S31	AO	LCD SEG31 output
					RXD3	I/O	UART3 data input or synchronous mode data output
					MISO	I/O	SPI master receive and slave send
					SCL	I/O	I^2C clock input and output
					PG5	O	PWM output channel 5
					CC0	O	Timer2 comparison output channel 0
-	-	-	16	-	P46	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S30	AO	LCD SEG30 output
					C0_O	O	ACMP0 output
					FB1	I	PWM external brake signal 1 input
					NRST	I	External reset
-	-	-	15	-	P47	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S29	AO	LCD SEG29 output
					NSS(NSSO3)	I/O	SPI slave select input or master select channel 3 output
					CAP3	I	Timer2 input capture channel 3
27	4	8	8	6	P50	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S24	AO	LCD SEG24 output
					PG0	O	PWM output channel 0
					C1_O	O	ACMP1 output
					ADET	I	ADC external trigger input
					OSCIN2	AI	External oscillation 2 input
28	5	9	9	7	P51	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S25	AO	LCD SEG25 output
					PG1	O	PWM output channel 1
					OSCOUT2	AO	External oscillation 2 output
1	6	10	10	8	P52	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers

Number					Function	Type	Description
CMS80F 26282	CMS80F 2629	CMS80F 262A	CMS80F 262B	CMS80F 262C			
					PG4	O	PWM output channel 4
					T0G	I	Timer0 gate control input
					NRST	I	External reset
-	7	11	11	9	P53	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S26	AO	LCD SEG26 output
					PG5	O	PWM output channel 5
					BUZZ	O	Buzzer output
					T0	I	Timer0 external clock input
-	-	-	13	-	P54	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S27	AO	LCD SEG27 output
					T1	I	Timer1 external clock input
-	-	-	14	-	P55	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
					LCD_S28	AO	LCD SEG28 output
					CC3	O	Timer2 comparison output channel 3
					T1G	I	Timer1 gate control input
2	8	12	12	10	VDD	P	Power supply
26	3	7	7	5	VSS	P	Ground

3.3 GPIO Features

Various functions of the pins are shared, and each I/O port can be configured as any digital function or specified analog function. As a general-purpose GPIO port, I/O has the following features:

- Configurable 2 levels of I/O output rate.
- Can read data latch status or pin status.
- Configurable rising edge, falling edge, both edge trigger interrupt.
- Configurable rising edge, falling edge, both edge interrupt to wake up the chip.
- Can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 Pin Function List

Digital function list:

	External input	Digital function configuration						
		0	1	2	3	4	5	6
P00	T1G, ADET	GPIO	ANA	-	-	-	PG3	-
P01	T0G	GPIO	ANA	-	-	-	PG2	-
P02	T0	GPIO	ANA	-	-	-	PG1	CC2
P03	T1	GPIO	ANA	-	-	-	PG0	C0_O
P04	T2EX, CAP0	GPIO	ANA	-	SCLK	SCL	PG5	-
P05	T2	GPIO	ANA	TXD2	MOSI	SDA	PG4	C1_O
P06	-	GPIO	ANA	RXD2	MISO	-	-	C0_O
P07	-	GPIO	ANA	-	NSS(NSSO0)	-	-	-
P10	ADET	GPIO	ANA	-	-	-	-	-
P11	-	GPIO	ANA	RXD1	MISO	-	-	-
P12	-	GPIO	ANA	-	SCLK	SCL	-	CLO
P13	-	GPIO	ANA	TXD1	MOSI	SDA	-	-
P14	-	GPIO	ANA	RXD1	MISO	SCL	-	-
P15	-	GPIO	ANA	-	NSS(NSSO1)	-	-	-
P16	-	GPIO	ANA	-	-	-	-	CC0
P17	T1G	GPIO	ANA	-	-	-	-	CC1
P20	T1, ADET	GPIO	ANA	RXD0	-	-	-	BUZZ
P21	-	GPIO	ANA	TXD0	-	-	PG1	-
P22	-	GPIO	ANA	RXD1	MOSI	-	PG0	-
P23	-	GPIO	ANA	TXD1	MISO	-	PG3	-
P24		GPIO	ANA	-	SCLK	-	PG2	-
P25	-	GPIO	ANA	-	NSS(NSSO2)	-	FB0	-
P26	-	GPIO	ANA	-	-	-	PG5	CLO
P27	CAP1	GPIO	ANA	-	-	-	PG4	-
P30	CAP2, ADET	GPIO	ANA	-	-	-	PG0	-
P31	-	GPIO	ANA	-	NSS(NSSO3)		PG1	-
P32	-	GPIO	ANA	-	-	-	PG2	-
P33	-	GPIO	ANA	-	-	-	PG3	-
P34	-	GPIO	ANA	-	-	-	PG4	-
P35	-	GPIO	ANA	-	-	-	PG5	-
P36	-	GPIO	ANA	-	-	-	-	-
P37	-	GPIO	ANA	-	-	-	-	C0_O
P40	ADET	GPIO	ANA	-	-	-	PG0	-
P41	-	GPIO	ANA	-	-	-	PG1	-
P42	-	GPIO	ANA	-	-	-	PG2	-
P43	-	GPIO	ANA	-	SCLK	SCL	PG3	CLO
P44	-	GPIO	ANA	TXD3	MOSI	SDA	PG4	-
P45	-	GPIO	ANA	RXD3	MISO	SCL	PG5	CC0
P46	-	GPIO	ANA	-	-	-	FB1	C0_O

P47	CAP3	GPIO	ANA	-	NSS(NSSO3)	-	-	-
P50	ADET	GPIO	ANA	-	-	-	PG0	C1_O
P51	-	GPIO	ANA	-	-	-	PG1	-
P52	T0G	GPIO	-	-	-	-	PG4	-
P53	T0	GPIO	ANA	-	-	-	PG5	BUZZ
P54	T1	GPIO	ANA	-	-	-	-	-
P55	T1G	GPIO	ANA	-	-	-	-	CC3

Led, analog function, CONFIG configuration list:

	GPIO(0)		ANA(1)				CONFIG
	LEDSEG	LEDCOM	ADC	LCDSEG	LCDCOM	ACMP	
P00	LED_S16	-	-	LCD_S16	-	-	-
P01	LED_S17	-	-	LCD_S17	-	-	-
P02	LED_S18	-	-	LCD_S18	-	-	DSCK2
P03	LED_S19	-	-	LCD_S19	-	-	DSDA2
P04	LED_S20	-	-	LCD_S20	-	C0P0	-
P05	LED_S21	-	-	LCD_S21	-	C0N0	-
P06	LED_S22	-	-	LCD_S22	-	C1P0	OSCIN1
P07	LED_S23	-	-	LCD_S23	-	C1N	OSCOUT1
P10	LED_S0	-	-	LCD_S0	-	-	-
P11	LED_S1	-	-	LCD_S1	-	-	DSDA1
P12	LED_S2	-	AN17	LCD_S2	-	-	-
P13	LED_S3	-	AN18	LCD_S3	-	-	DSCK1
P14	LED_S4	-	AN0	LCD_S4	-	-	-
P15	LED_S5	-	AN1	LCD_S5	-	-	-
P16	LED_S6	-	AN2	LCD_S6	-	-	-
P17	LED_S7	-	AN3	LCD_S7	-	-	-
P20	LED_S8	-	AN4	LCD_S8	-	-	-
P21	LED_S9	-	AN5	LCD_S9	-	-	-
P22	LED_S10	-	AN6	LCD_S10	-	-	-
P23	LED_S11	-	AN7	LCD_S11	-	-	-
P24	LED_S12	-	AN19	LCD_S12	-	-	-
P25	LED_S13	-	AN20	LCD_S13	-	-	-
P26	LED_S14	-	AN21	LCD_S14	-	-	-
P27	LED_S15	-	AN22	LCD_S15	-	-	-
P30	LED_S27	LED_C0	-	LCD_S39	LCD_C0	-	-
P31	LED_S26	LED_C1	-	LCD_S38	LCD_C1	-	-
P32	LED_S25	LED_C2	-	LCD_S37	LCD_C2	-	-
P33	LED_S24	LED_C3	-	LCD_S36	LCD_C3	-	-
P34	-	LED_C4	AN8	LCD_S35	LCD_C4	-	-
P35	-	LED_C5	AN9	LCD_S34	LCD_C5	-	-
P36	-	LED_C6	AN10	LCD_S33	LCD_C6	-	-
P37	-	LED_C7	AN11	LCD_S32	LCD_C7	-	-

P40	-	-	AN12	-	-	C0P4	-
P41	-	-	AN13	-	-	C0P5	-
P42	-	-	AN14	-	-	C0P6	-
P43	-	-	AN15	-	-	C0P7	-
P44	-	-	AN16	-	-	C0N1	-
P45	-	-	-	LCD_S31	-	-	-
P46	-	-	-	LCD_S30	-	-	NRST
P47	-	-	-	LCD_S29	-	-	-
P50	-	-	-	LCD_S24	-	-	OSCIN2
P51	-	-	-	LCD_S25	-	-	OSCOUT2
P52	-	-	-	-	-	-	NRST
P53	-	-	-	LCD_S26	-	-	-
P54	-	-	-	LCD_S27	-	-	-
P55	-	-	-	LCD_S28	-	-	-

4. Function Summary

4.1 System Clock

The system clock has 4 clock sources, which can be selected through the system configuration register settings. The system clock can be selected from the following 4 types:

- Internal high-speed oscillator HSI (48MHz).
- External high-speed oscillator HSE (8MHz/16MHz).
- External low-speed oscillator LSE (32.768KHz).
- Internal low-speed oscillator LSI (125KHz).

4.2 Reset

The reset operation is used to complete the initialization of the internal circuit of the chip, so that the system starts working from a certain state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low-voltage reset.
- Watchdog overflow reset.
- Window watchdog reset.
- Software reset.
- CONFIG state protection reset.
- Power-on configuration monitoring reset.

Any of the above reset situations requires a certain response time, and the system provides a complete reset process to ensure the smooth progress of the reset action.

4.3 Power Management

4.3.1 Operating Mode

The chip has 4 different working modes to meet the power consumption requirements of different applications.

- Normal working mode

  MCU is in normal working state and peripherals are operating normally.

- Idle mode 1 (IDLE 1)

  MCU is in idle mode 1(IDLE1), CPU stops working, both digital and analog peripherals are operating normally. This mode can be awakened by any interrupt.

- Idle mode 2 (IDLE 2)

  MCU is in idle mode 2(IDLE1), CPU stops working, and digital peripherals are operating normally, but the analog peripherals (ADC/ACMP/ADC-LDO) enable bit will be forcibly disabled. This mode can be awakened by any interrupt except ADC interrupt and ACMP interrupt.

- Sleep mode STOP

  MCU is in sleep mode, CPU stops working, both digital and analog peripherals stop working. This mode can be awakened by INT0/1, external interrupt, WUT timer, LSE timer, WWDT timer.

4.3.2 Power Supply Low-voltage Reset (LVR)

When the power supply voltage is lower than the set detection voltage, the system resets.

There are 4 options for low voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Power Supply Low-voltage Detection (LVD)

The low voltage detection circuit compares the power supply voltage with the set voltage, and if the power supply voltage is lower or higher than the set voltage, an trigger request signal is generated.

There are 16 options for the settable detection voltage: 2.0V ~ 4.6V.

4.4 Interrupt control

The chip has multiple interrupt sources and interrupt vectors. The user-settable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer, PWM, I2C, SPI, UART0/1/2/3, P0/P1/P2/P3/P4/P5, ACMP0/1, ADC, WWDT, the actual number of interrupt sources varies by product.

The chip stipulates two interrupt priority levels, which can realize two-level interrupt nesting. When an interrupt has been responded, if a high-level interrupt sends a request, the latter can interrupt the former to achieve interrupt nesting.

4.5 Timer

4.5.1 Watch Dog Timer (WDT)

The watchdog timer is an on-chip timer whose clock source is provided by the system clock. The WDT timeout will generate a reset. The watchdog reset is a protection setting of the system. When the system runs to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an infinite loop. The WDT timer has the following characteristics:

- 8 levels of watchdog overflow time are selectable.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 Window WatchDog Timer (WWDT)

Window watchdog timer is a 5-bit down-counting timer with clock source provided by LSI and selectable frequency division. By clearing the timer in the specified window, the system can be prevented from entering an infinite loop due to an error state. The timer can generate interrupts, wake up the system in sleep mode, and reset the chip. The WWDT timer has the following characteristics:

- 5 levels of window comparison time are selectable.
- Window watchdog overflow interrupt can be set.
- Window watchdog overflow reset can be set.

4.5.3 Timer Counter 0/1 (Timer0/1)

Timer 0 is similar in type and structure to Timer 1, and is two 16-bit up-counting timers. Timer0 has 4 working modes, Timer1 has 3 working modes, they provide basic timing and event counting operations.

In "timer mode", the timer register is incremented every 12 or 4 system cycles when the timer clock is enabled. In the "counter mode", the timing register will increase whenever it detects a falling edge on the corresponding input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- Can be used for gated counting function.
- Counter overflow interrupt.

4.5.4 Timer Counter 2 (Timer2)

Timer 2 is a 16-bit timer, which can be used for various digital signal generation and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following characteristics:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- With reload prohibition, overflow auto-reload, external pin falling edge auto-reload function.
- Capture can be triggered by rising edge, falling edge, both edges or writing the low byte of the capture register.
- With a comparison function, this function can generate a periodic signal and a PWM waveform with a controllable duty cycle.
- Interrupts can be generated by timer, external trigger, capture or comparison.
- Support continuous capture mode.

4.5.5 Timer 3/4 (Timer3/4)

Timer 3/4 is similar to timer 0/1 and is two 16-bit timers. Timer3 has 4 working modes, and Timer4 has 3 working modes. Compared with Timer0/1, Timer3/4 only provides timing operation.

When the timer is started, the value of the register (counter) is incremented every 12 or 4 system cycles.

4.5.6 LSE Timer

The LSE timer is a 16-bit up-counting timer with a clock source from the external low-speed clock LSE. The LSE timer has the following characteristics:

- Timing function.
- 16-bit timing value can be set.
- Can work normally in sleep mode.
- An interrupt can be generated when the count value is equal to the timer value.
- Timed interrupt can wake up idle mode 1/idle mode 2/sleep mode.

4.5.7 Wake-up Timer (WUT)

WUT wake-up timer is a 12-bit, up-counting timer used for wake-up from sleep and a clock source from the internal low-speed clock LSI. After the system enters the sleep mode, the CPU and all peripheral circuits stop working, and the internal low-speed clock LSI provides the clock for the WUT counter. WUT has the following characteristics:

- The system can be woken up regularly in sleep mode.
- Count clock can be divided by 1, 8, 32, 256.
- 12-bit timing value can be set.

4.5.8 Baud Rate Timer (BRT/BRT1)

The BRT and BRT1 timers are 16-bit baud rate timers whose clock source comes from the system clock. They mainly provide clocks for the UART module. BRT/BRT1 has the following characteristics:

- With independent control switch.
- Counting clock has 8 frequency division options.
- 16-bit up counting.

4.6 Enhanced Digital Peripherals

4.6.1 BUZZER

The buzzer driver is composed of an 8-bit counter, a clock driver, and a control register. It outputs a square wave with a duty cycle of 50%, and its frequency covers a wide range. BUZZER has the following characteristics:

- With separate enable control switch.
- A total of 4 levels of system clock divider ratios of 8, 16, 32, 64 can be set.
- Output frequency divider can be set (1~255) x 2 through 8-bit register.

4.6.2 Cyclic Redundancy Check (CRC)

CRC is a commonly used error-detecting code. The main feature is that any choice of length of information data and verification data is possible. CRC verification unit generates polynomial '$X^{16}+X^{12}+X^5+1$'(CRC-16-CCITT). The data that needs to be checked is selected from programs, therefore this module is not only used in program flashspace but many other places.

4.6.3 Multiplication and Division Unit (MDU)

The MDU module has the following characteristics:

- Support 32bit/16bit division.
- Support 16bit/16bit division.
- Support 16bit×16bit multiplication.
- Support 32 bit shift operation.
- Support normalization operation.

4.6.4 Enhanced PWM Module

The enhanced PWM module supports 6 PWM generators, and the period and duty cycle can be set independently. PWM has the following characteristics:

- Support 2 kinds of waveform output in single and continuous mode.
- Support 4 control modes: independent, complementary, synchronous and group control.
- Count clock can be divided by 1, 2, 4, 8, 16.
- Support two counting modes: edge alignment and center alignment, symmetrical and asymmetrical counting are supported in center alignment mode.
- Support mask output.
- Support dead zone programming.
- Output polarity can be set.
- Support cycle, compare up, compare down, zero interrupt.
- Support software brake, external port trigger brake, ADC comparison result trigger brake, ACMP output trigger brake.
- Support 4 kinds of fault recovery modes.

4.7 Display Interface

4.7.1 Hardware LCD Driver Module

The LCD drive module includes a controller, a duty cycle generator, COM and SEG output ports. The module has the following characteristics:

- Up to 8 COM ports and 32 SEG ports.
- Support two modes of traditional resistance and fast charging.
- The fast charging time is optional.
- Support contrast adjustment.
- Optional bias voltage: 1/2, 1/3, 1/4.
- The duty cycle is optional: 1/4, 1/5, 1/6, 1/8.
- The clock source is optional: system clock, LSI, LSE.

4.7.2 Hardware LED Drive Module

The LED drive module can easily realize the display drive of the LED. The module has the following characteristics:

- 1/4, 1/5, 1/6, 1/8 four kinds of DUTY are optional.
- System clock, LSI, LSE three clock sources are optional
- 16-bit clock source frequency divider controller.
- Two driving modes of common cathode and common anode for COM port are optional.
- Supports up to 8 COM ports and 24 SEG ports.
- The COM port current 50mA and 150mA are two options (VOL=1.5V@VDD=5V).
- The SEG port current can be selected in 16 levels, and the maximum current can reach 40mA (VOH=3.5V@VDD=5V).

4.8 Communication Module

4.8.1 SPI Module

SPI is a fully configurable SPI master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it can also communicate between processors in a multi-host system. SPI has the following characteristics:

- Full-duplex synchronous serial data transmission.
- Support master/slave mode.
- Support multi-host system.
- System error detection.
- Support speed up to 1/4 of the system clock (FSYS≤24MHz).
- Bit rate generates 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Support four transmission formats.
- Send/receive complete can generate interrupt.

4.8.2 I²C Module

The two-wire bidirectional serial bus controller I2C provides a simple and effective connection method for data exchange between the microprocessor and the I2C bus. The I2C module has the following characteristics:

- Support 4 working methods: master sending, master receiving, slave sending, slave receiving.
- Support 2 transmission speed modes:
  Standard (up to 100Kb/s);
  Fast (up to 400Kb/s).
- Perform arbitration and clock synchronization.
- Support multi-host system.
- The host method supports 7-bit addressing mode and 10-bit addressing mode on the I2C bus (software support).
- The slave method supports 7-bit addressing mode on the I2C bus.
- Allows operation in a wide range of clock frequencies (built-in 8-bit timer).
- An interrupt can be generated when receiving/sending is complete.

4.8.3 UARTn Module

UARTn module contains UART0/ UART1/ UART2/ UART3, 4 serial ports with exactly the same function. UARTn has the following characteristics:

- Full-duplex serial port.
- Support synchronous mode.
- Support 8-bit asynchronous transceiver mode with variable baud rate.
- Support 9-bit asynchronous transceiver mode with variable baud rate.
- Baud rate can be generated by Timer1/Timer4/Timer2/BRT/ BRT1 module.
- Send/receive complete can generate interrupt.

4.9 Analog Module

4.9.1 Analog to Digital Conversion (ADC)

ADC module is a 12-bit successive approximation analog-to-digital converter. The port analog input signal is connected to the input of the analog-to-digital converter after passing through the multiplexer. The analog-to-digital converter generates a 12-bit binary result according to the input analog signal and saves the result in the ADC result register. ADC has the following characteristics:

- Up to 23 external channels.
- ADC conversion clock has 8 clock frequencies to choose from.
- ADC reference voltage can choose 2.0V/2.4V/3.0V/VDD.
- A complete 12-bit conversion requires 18.5 ADC conversion cycles.
- Support external port edge, enhanced PWM trigger ADC conversion.
- Support ADC conversion result comparison output, comparison output can control enhanced PWM brake function.
- Support ADC conversion completion to generate interrupt.

4.9.2 Analog Comparator (ACMP0/1)

The comparators ACMP0 and ACMP1 have the following characteristics:

- The positive end supports multiple input ports optional.
- The negative terminal can select port input or internal reference voltage.
- The internal reference voltage divider has a total of 16 gear selections.
- Support output filtering, a total of 11 filter time options.
- Support unilateral and bilateral hysteresis control.
- Hysteresis voltage optional 10/20/60mV.
- Support offset voltage through software trimming.
- The output can be used as an enhanced PWM brake trigger signal.
- Support output change to generate interrupt.
- Supports output latching.

4.10 FLASH Memory

FLASH memory includes program memory (APROM) and non-volatile data memory (Data FLASH), which can be accessed through related special function registers (SFR) to realize IAP function. FLASH memory supports the following operations:

- Byte read operation.
- Byte write/ Continuously write operation.
- Page erase operation.

4.11 Unique ID (UID)

Each chip has a 96-bit unique identification number, namely Unique identification. The UID has been set at the factory and cannot be modified by the user.

5. User Configuration

The system configuration register (CONFIG) is the FLASH option of the MCU's initial conditions, and the program cannot access and operate it. The following contents can be set through the system configuration register:

- Watchdog's working method.
- FLASH program area partition protection, code encryption, FLASH data area partition protection, encryption status.
- Low voltage reset voltage.
- Disable or enable debug mode.
- Oscillation method, prescaler selection.
- Internal high-speed oscillator frequency division selection.
- External reset configuration, port selection.
- Sleep wake-up waiting time.

6. Electrical Characteristics

(TA=25℃, Unless otherwise indicated)

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	200	mA
I_{IO}	Maximum sink current of a single IO	-	50	mA
	Maximum sink current of a single IO（LED_COM）	-	150	mA
	Maximum source current of a single IO	-	40	mA
	Maximum source current of a single IO（LED_SEG）	-	40	mA
	Maximum sink current of all IOs	-	200	mA
	Maximum source current of all IOs	-	120	mA

Note: If the operating conditions of the device exceed the absolute maximum rating range, the device will be permanently damaged. Function is guaranteed only if the device operates within the limits specified in the manual. The absolute maximum rating of chips may affect the reliability of devices.

6.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V, T_A=25℃

Symbol	Parameter	Test condition	Min.	Typ.	Max.	unit
VDD	Operating voltage	F_{SYS}=48MHz, machine cycle=2T F_{SYS}=24MHz, machine cycle=1T F_{SYS}=8MHz~16MHz, machine cycle=1T	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals are off machine cycle=2T	-	9	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals are off machine cycle=2T	-	9	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off machine cycle=1T	-	6	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off machine cycle=1T	-	6	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off machine cycle=1T	-	5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off machine cycle=1T	-	5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals are off machine cycle=1T	-	3.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off machine cycle=1T	-	3.5	-	mA
	IDLE1	VDD=5V, F_{SYS}=48MHz, all peripherals are off	-	7.5	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals are off	-	7.5	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off	-	5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off	-	5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off	-	4	-	mA

		VDD=3V, F_{SYS}=16MHz, all peripherals are off	-	4	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals are off	-	3	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off	-	3	-	mA
	IDLE2	VDD=5V, F_{SYS}=125KHz, all peripherals are off	-	21	-	uA
		VDD=3V, F_{SYS}=125KHz, all peripherals are off	-	21	-	uA
		VDD=5V, F_{SYS}=32.768KHz, all peripherals are off	-	22	-	uA
		VDD=3V, F_{SYS}=32.768KHz, all peripherals are off	-	14	-	uA
I_{SLEEP1}	Sleep current	VDD=3V, All peripherals are off, LSE/LSE timer enable	-	16	-	uA
I_{SLEEP2}	Sleep current	VDD=3V, All peripherals are off, LSI/WUT timer enable	-	8	-	uA
I_{SLEEP3}	Sleep current	VDD=3V, All peripherals are off	-	6	-	uA
I_{LI}	Input leakage	-	-1	-	1	uA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
V_{OL}	Output Low voltage	VDD=5V, I_{OL1}=18mA	-	-	0.4	V
		VDD=5V, I_{OL2}=50mA (LED_COM)	-	-	0.4	V
		VDD=3V, I_{OL1}=12mA	-	-	0.4	V
		VDD=3V, I_{OL2}=36mA (LED_COM)	-	-	0.4	V
V_{OH}	High output voltage	VDD=5V, I_{OH1}=35mA	3.5	-	-	V
		VDD=5V, I_{OH2}=35mA (LED_SEG Max)	3.5	-	-	V
		VDD=5V, I_{OH3}=2.5mA (LED_SEG Min)	3.5	-	-	V
		VDD=3V, I_{OH1}=14mA	2.1	-	-	V
		VDD=3V, I_{OH2}=14mA (LED_SEG Max)	2.1	-	-	V
		VDD=3V, I_{OH3}=1mA (LED_SEG Min)	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC Electrical Parameters

6.3.1 Power-up and Power-down Time

TA=25℃, Not include 32.768K crystal oscillator start-up time.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External Oscillator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HSE}	Operating voltage	F=8/16MHz, C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz, C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

Symbol	Parameter	Condition	Frequency error range	Min.	Typ.	Max.	Unit
F_{HSI}	Internal high speed oscillator 48MHz	T_A = 25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal low speed oscillator 125KHz	T_A=25℃	±20%	-	125	-	KHz
		T_A=-40℃ to 105℃	±50%	-	125	-	KHz

6.3.4 Low-voltage Reset Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVR1}	Low voltage detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low voltage detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low voltage detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low voltage detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 Low-voltage Detection Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVD1}	Low voltage detection threshold 2.00V	1.90	2.00	2.10	V
V_{LVD2}	Low voltage detection threshold 2.15V	2.05	2.15	2.25	V
V_{LVD3}	Low voltage detection threshold 2.30V	2.20	2.30	2.40	V
V_{LVD4}	Low voltage detection threshold 2.45V	2.35	2.45	2.55	V
V_{LVD5}	Low voltage detection threshold 2.60V	2.50	2.60	2.70	V
V_{LVD6}	Low voltage detection threshold 2.75V	2.65	2.75	2.85	V
V_{LVD7}	Low voltage detection threshold 2.90V	2.80	2.90	3.00	V
V_{LVD8}	Low voltage detection threshold 3.05V	2.95	3.05	3.15	V
V_{LVD9}	Low voltage detection threshold 3.20V	3.10	3.20	3.30	V
V_{LVD10}	Low voltage detection threshold 3.40V	3.30	3.40	3.50	V
V_{LVD11}	Low voltage detection threshold 3.60V	3.50	3.60	3.70	V
V_{LVD12}	Low voltage detection threshold 3.80V	3.70	3.80	3.90	V
V_{LVD13}	Low voltage detection threshold 4.00V	3.90	4.00	4.10	V
V_{LVD14}	Low voltage detection threshold 4.20V	4.10	4.20	4.30	V
V_{LVD15}	Low voltage detection threshold 4.40V	4.30	4.40	4.50	V
V_{LVD16}	Low voltage detection threshold 4.60V	4.50	4.60	4.70	V

6.4 FLASH Electrical Parameter

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	25	105	℃
$N_{ENDURANCE}$	Number of erasing and writing	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	1.5	-	ms
T_{WRITE}	Byte write time	-	-	30	-	us
T_{READ}	Read time	-	-	3*Tsys	-	-
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

6.5 Analog Characteristics

6.5.1 BANDGAP Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal 1.2V	VDD=2.1~5.5V、T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V、T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V、T_A=-40℃ to 105℃	1.176	1.2	1.224	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2		1.99	2.0	2.01	V
V_{REF3}	Reference voltage 3		2.39	2.4	2.41	V
V_{REF4}	Reference voltage 4		2.99	3.0	3.01	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	Resolution		12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)		±2			LSB
INL	Integral nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)		±4			LSB
T_{ADCK}	ADC clock cycle	V_{REF}=VDD=5V	0.5	-	-	us
		V_{REF} =V_{REF2}/ V_{REF3}/V_{REF4}	2	-	-	us
T_{ADC}	ADC conversion time		-	18.5	-	T_{ADCK}
F_S	Sampling rate (V_{REF}=V_{AVDD}=5V)		100			Ksps

6.5.3 ACMP Electrical Characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	No calibration (CnCON1[4:0] =10H)	-	±4.0	-	mV
		After calibration	-	±0.5	±1.0	
V_{CM}	Common-mode input range	-40℃ ~105℃	-0.1	-	VDD-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃ ~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃ ~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open-loop voltage gain	-	-	90	-	dB
BW	Bandwidth	-	-	200	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V -40℃ ~105℃	-	100	-	dB
Transient characteristics						
T_{STB}	Stable time	-	-	-	5	us
T_{PGD}	Response delay time	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

6.6 EMC Characteristics

6.6.1 EFT Electrical Characteristics

Symbol	Parameter	Condition	Rank
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDD and VSS pins to induce a functional disturbance	T_A = + 25°C, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4B

Note: The electrical fast transient burst (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.) The EFT parameters in the above table are the results measured on the internal test platform of the CMS, and are not applicable to all application environments. The test data is only for reference. All aspects of system design may affect the EFT performance. In applications with high EFT performance requirements, attention should be paid to avoid interference sources affecting the system operation as much as possible. It is recommended to analyze the interference path and optimize the design to achieve the best anti-interference performance.

6.6.2 ESD Electrical Characteristics

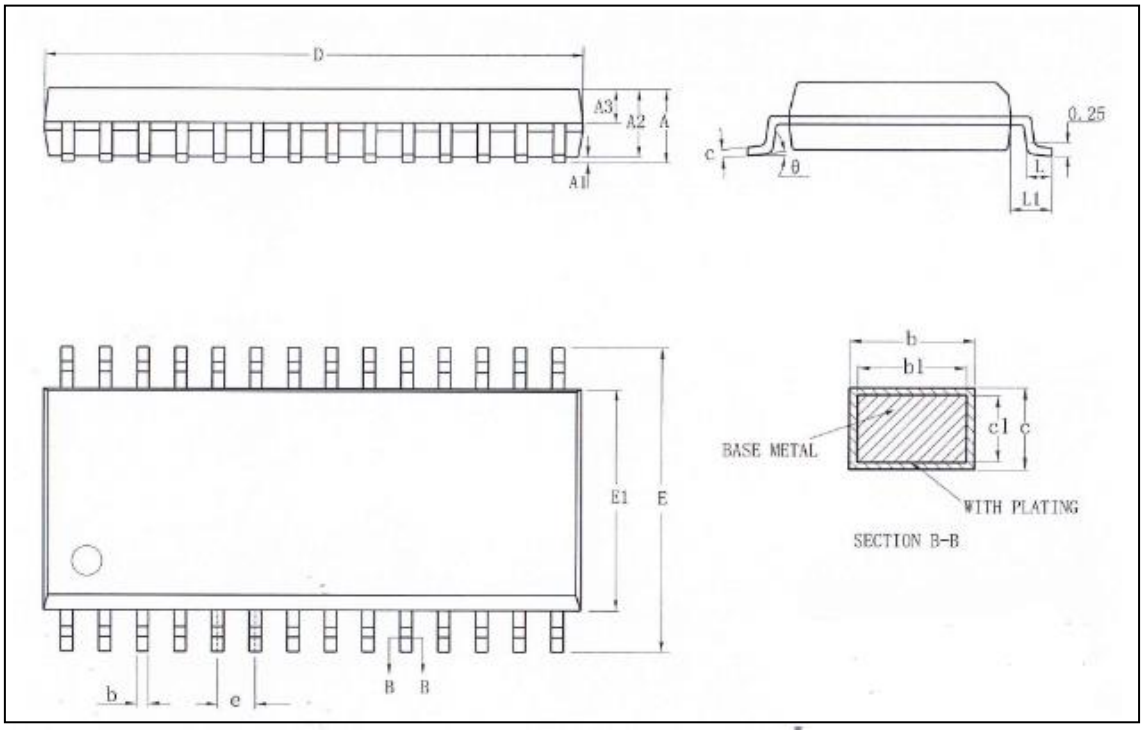
Symbol	Parameter	Condition	Rank
V_{ESD}	Electrostatic discharge (Human body discharge mode - HBM)	T_A = + 25°C, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine discharge mode - MM)	T_A = + 25°C, JEDEC EIA/JESD22- A115	C

6.6.3 Latch-up Electrical Characteristics

Symbol	Parameter	Condition	Class
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25°C)

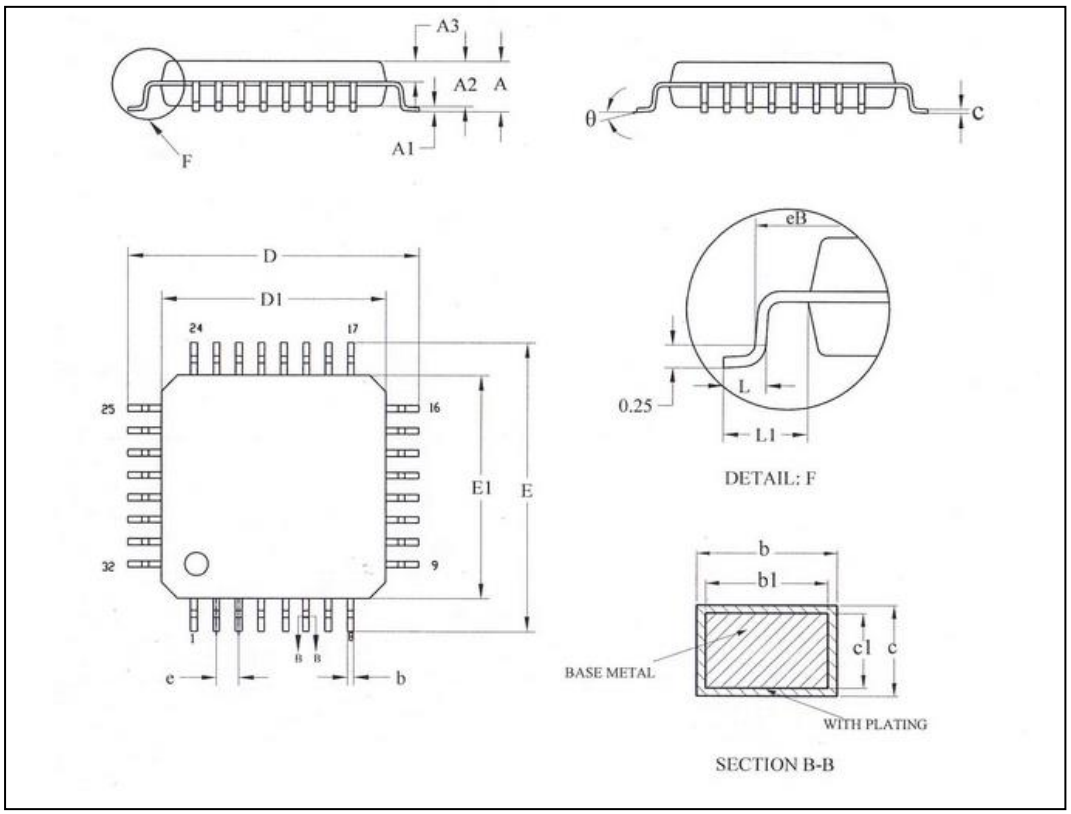
7. Package Information

7.1 SOP28



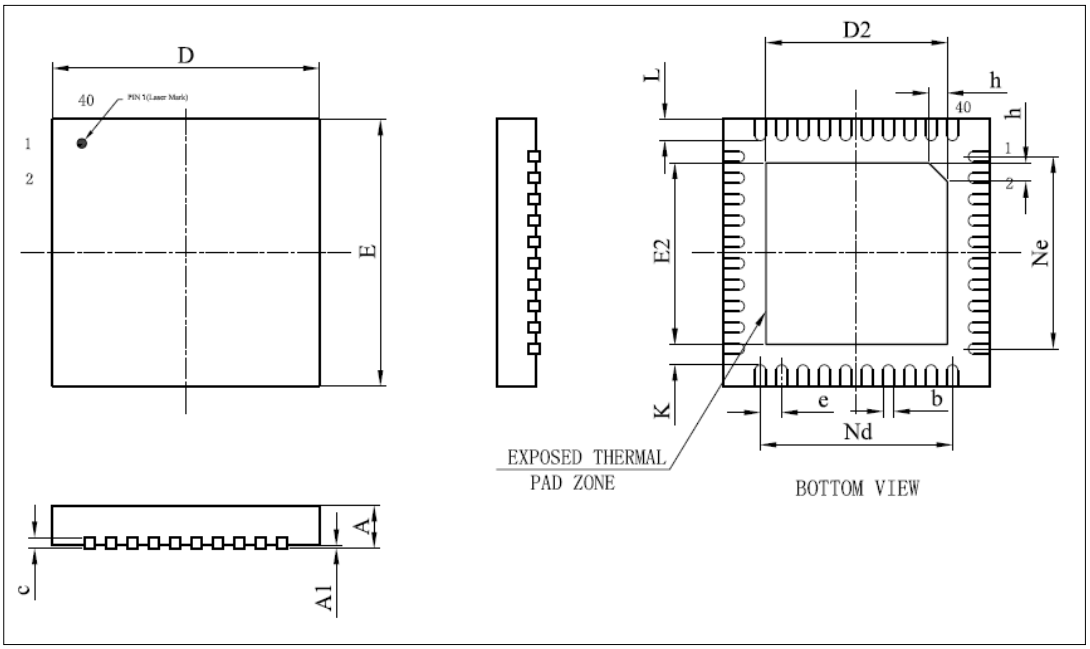
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.2 LQFP32



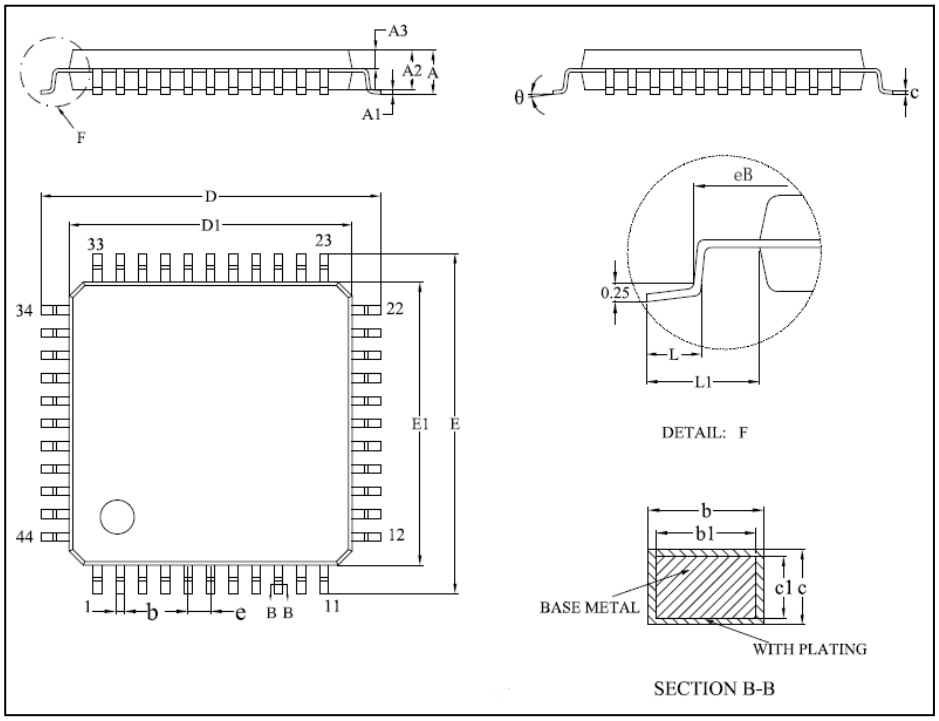
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.3 QFN40



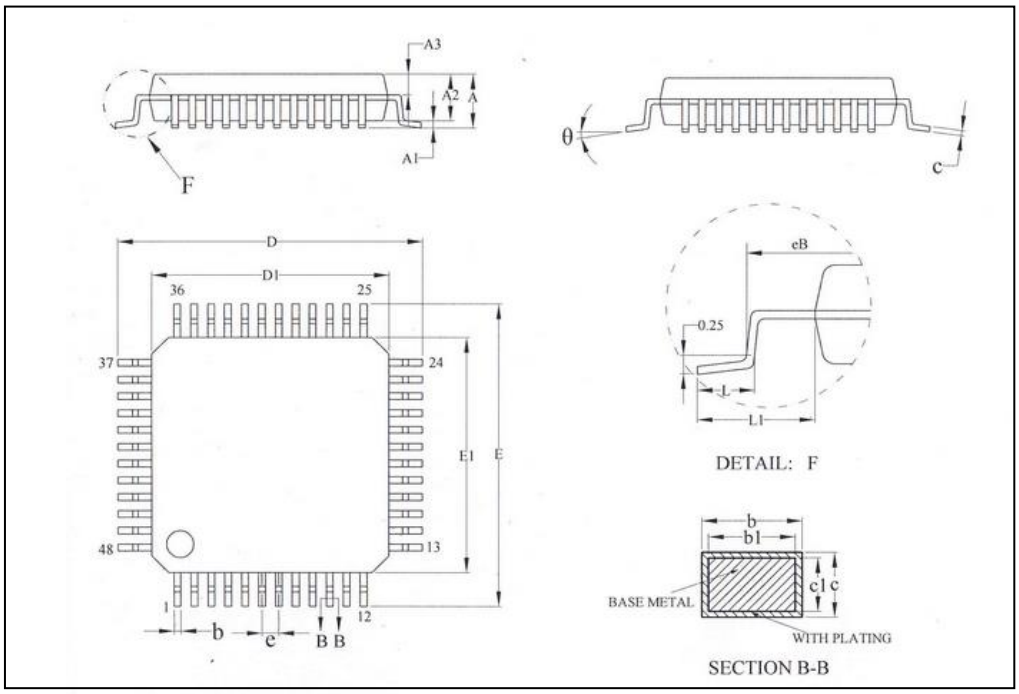
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	-	-
h	0.30	0.35	0.40

7.4 LQFP44



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
eB	11.05	-	11.25
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

7.5 LQFP48



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

8. Revision History

Revision	Date	Modify content
V1.00	Jun 2021	Initial verison
V1.01	Apr 2022	1) 6.1 Absolute maximum ratings: added notes on limit parameters 2) 6.2 DC electrical characteristics: modified parameters 3) 6.3.3 internal oscillatorInternal: modified parameters 4) 6.5.1 BANDGAP electrical characteristics: adjusted 5) 6.5.2 ADC electrical characteristics: adjusted ADCclock cycles according to different reference voltages
V1.02	Jul 2022	1) 4.3.3 Power Supply Low-voltage Detection (LVD), 2) 4.4 Interrupt control: adjust description 3) Added CMS80F26282/CMS80F262C model and related description
V1.03	Sep 2022	3.1.2 CMS80F2629 Pin Diagram: Correct the error label DSCK1I to DSCK1
V1.0.4	Apr 2023	1) Update 6.6EMC Characteristics 2) Correct the packaging dimensions of 7.2LQFP32 and 7.4LQFP44